

PATENT
IBM Docket No. FR920000082US1

Amendments to the Specification:

Please modify the paragraph beginning on page 2 at line 1 as follows:

The shared memory switch is a device wherein the packets received by the input ports are stored into a memory at locations the addresses of which are determined by queues containing the packet destination addresses, the packets being transmitted on the output ports as the destination addresses are dequeued. Although such a switch ~~enables to~~ incurs a very low cell-lost rate, it presents a bottleneck due to the requirement of the memory bandwidth, the segregation of the memory space and the centralized control of the memory which causes the switch performance to degrade as the size of the switch increases. A traditional approach to design a large shared memory switch has been to first design a feasible size shared memory switch and then to interconnect a plurality of such modules in order to build a large switch. This general scheme of switch growth is known to cause degradation in performance of shared memory architecture as the switch grows in size insofar as the memory access controller will have to increase the number of all centralized control functions and memory operations thereby reducing drastically the access to the shared memory. A growable switch approach packet switch architecture is a plurality of shared memory switches organized in a single stage preceded by a buffer-less interconnection network. This approach does not allow global sharing of memory space along all its inputs and outputs. It is known that this approach does not provide the best memory utilization as possible for a memory belonging to a group of output ports to overflow under unbalanced or bursty traffic conditions.

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Please modify the paragraph beginning on page 3 at line 25 as follows:

Accordingly, the main object of the invention is to provide a packet switch wherein the multicast function does not require to use of multicast routing tables for the duplication of the memory addresses or to duplicate the requests to send.

Please modify the paragraph beginning on page 3 at line 30 as follows:

The invention relates, therefore, to a data transmission system comprising a plurality of Local Area Networks (LANs) interconnected by a hub including the same plurality of LAN adapters respectively connected to said LANs and a packet switch comprising at least a packet switch module interconnecting all LAN adapters wherein a packet transmitted by any adapter to the packet switch includes a header containing at least the address of the adapter to which the packet is forwarded. The switch module comprises a plurality of input ports and a plurality of output ports both being respectively connected to the LAN adapters, each couple of an input port and an output port defining a crosspoint within the switch module. The system comprises a memory block located at each crosspoint of the switch module, which ~~includes~~ includes memory control means for determining from the header of the received data packet whether the packet is to be forwarded to the output port associated with the crosspoint and a data memory unit for storing at least the data packet into the data memory unit before sending it to the output port in such a case. The memory control means analyzes all the bytes following the header when the header includes a specific configuration indicating that the packet is a multicast address packet preceding a multicast frame in order to determine whether the packets of the multicast frame are to be forwarded to the output port corresponding to the memory block.

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Please modify the paragraph beginning on page 4 at line 24 as follows:

The above and other objects, features and advantages of the invention will be better understood by reading the following more particular description of the invention in conjunction with the accompanying drawings wherein :

- Fig. 1 is a schematic block diagram of a data transmission system including four LANs interconnected by a hub according to the principles of the invention.
- Fig. 2 represents schematically a data packet with the header of two bytes added by the adapter which is transmitted through a packet switch according to the invention.
- Fig. 3 is a block diagram representing the features of the packet switch being used in the packet data flow.
- Fig. 4 is a block diagram representing an input control block of the packet switch.
- Fig. 5 is a block diagram representing a memory block located at each crosspoint of the packet switch.
- Fig. 6 is a block diagram representing an input expansion data block of the packet switch.
- Fig. 7 is a block diagram representing an output data block of the packet switch.
- Fig. 8 is a block diagram representing the complete architecture of the packet switch.
- Fig. 9 is a flow chart representing the steps controlled by the scheduler when a single or multiple overflow occur.
- Fig. 10 is a schematic representation of a ~~multicast~~ multicast frame preceded by a multicast address packet which is transmitted to four output ports within three different packet ~~switch~~ switch modules.